Group III, claim 20.

Applicants also provisionally elected to prosecute Group II, including claims 13-16.

II. Response to Claim Rejections under 35 U.S.C. §§102 and 103

The Examiner conducted examination on the merits of the provisionally elected group II claims 13-16. In the Office Action, the Examiner rejected claims 13-14 under 35 U.S.C. §102(b) as being anticipated by Matsui et al. (U.S. Patent No. 5,589,029) and rejected claims 15-16 under 35 U.S.C. §103(a) as being unpatentable over Matsui et al. in view of Satoh (U.S. Patent No. 6,338,980), or Ohuchi (U.S. Patent No. 6,107,164), or Riding et al. (U.S. Patent No. 6,083,811).

Applicants respectfully traverse the rejections under 35 U.S.C. §§102 and 103.

The present invention is related to a semiconductor packaging technique.

Particularly, claim 13 recites a method of manufacturing a semiconductor device that, among other things, includes a step of peeling chips off an adhesive tape.

Matsui et al. discloses a semiconductor chip-supply apparatus that peels a chip off an adhesive sheet and transports the chip with a sucking member.

Satoh discloses a chip-scale package manufacturing method that includes forming a plurality of pads on an active face of an IC wafer, forming electrodes on the pads, dividing the wafer into pieces, applying protective resin on the active face of the wafer, applying an adhesive member on the active face, grinding an inactive face of the wafer, applying an adhesive member on the inactive face, dicing the protective resin, and removing the adhesive member.

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Ohuchi discloses a method of manufacturing a semiconductor device that includes forming protruded electrodes on a plurality of chip areas of a wafer, defining grooves in boundary regions of the chip areas, covering the wafer surface with a resin, polishing the back of the wafer to expose the grooves from the back, and dividing the wafer into pieces.

Riding et al. teaches a method for producing a thin dice from fragile materials that includes making saw cuts in a front surface of a body of fragile material defining the thin dice, applying a support film to the front surface, and grinding the back surface to expose the saw cuts.

The rejection of claims 13-14 under 35 U.S.C. §102(b) as being anticipated by Matsui et al. is respectfully traversed because, in order to properly anticipate Applicants' claimed invention under 35 U.S.C. §102(b), each and every element of the claim in issue must be found, either expressly described or under principles of inherency, in a single prior art reference. Furthermore, "[t]he identical invention must be shown in as complete detail as is contained in the . . . claim." See M.P.E.P. §2131 (8th ed., Aug. 2001), quoting *Richardson v. Suzuki Motor Co.*, 868 F.2d 1126, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). Finally, "[t]he elements must be arranged as required by the claim." M.P.E.P. §2131 (8th ed. 2001), p. 2100-69. Applicants submit that Matsui et al. does not disclose each and every element of the present invention as recited in claim 13.

Independent claim 13 recites, among other things, a step of peeling a chip off an adhesive tape that includes "thrusting the chip using pins from a back side of the adhesive tape with the adhesive tape between the chip and the pins, and keeping the

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pins at a peak position for an amount of time to facilitate peeling the chip off the adhesive tape, wherein the pins do not pierce the adhesive tape".

In contrast to the recitations in claim 13, <u>Matsui et al.</u> requires that in the step of peeling a chip off the adhesive sheet 2, "each upper end of the push-up needles 10 <u>pierces</u> the adhesive sheet 2 while the adhesive sheet 2 is moving downward" (col. 4, lines 2-4, emphasis added). <u>Matsui et al.</u> therefore fails to teach or suggest the feature of "the pins do not pierce the adhesive tape" as recited in claim 13 and clearly teaches away from the claimed invention.

In view of the above deficiencies of <u>Matsui et al.</u>, Applicants respectfully request that the rejection of claim 13 under 35 U.S.C. §102(b) be withdrawn, placing claim 13 in an allowable condition.

Claim 14, which depends from independent claim 13, is therefore also allowable at least because of its dependency from an allowable base claim.

The Examiner further combined <u>Matsui et al.</u> with <u>Satoh</u>, <u>Ohuchi</u> and <u>Riding et al.</u> to reject claims 15-16 under 35 U.S.C. §103(a). Applicants respectfully traverse this rejection, since a *prima facie* case of obviousness has not been made by the Examiner.

To establish a *prima facie* case of obviousness under 35 U.S.C. 103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element recited in the claims. (See M.P.E.P. §2143.03 (8th ed. 2001).) Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover,

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each of the these requirements must "be found in the prior art, and not be based on applicant's disclosure." (M.P.E.P. § 2143 (8th ed. 2001)

First, as discussed above, <u>Matsui et al.</u> fails to teach or suggest all of the steps recited in independent claim 13 and actually teaches away from claim 13.

On the other hand, <u>Satoh</u> discloses a manufacturing method of a chip-scale package that includes removing the first, second and third tapes. And in the steps of removing these tapes, <u>Satoh</u> only requires "the first adhering tape 3A . . . is removed" (col. 6, lines 7-8), "the second adhesive tape 3B . . . is removed" (col. 6, lines 26-27), and "the third adhesive tape 3C . . . is removed" (col. 6, lines 41-43). <u>Satoh</u> does not teach how to remove a chip from an adhesive tape, and therefore, <u>Satoh</u> does not overcome the above-mentioned deficiency of <u>Matsui et al.</u>

Similarly, neither <u>Ohuchi</u> nor <u>Riding et al.</u> teaches or discloses a method of peeling a chip off an adhesive tape. Both references are related to a wafer dicing method, not a chip pickup method. Obviously, neither of them overcomes the deficiency of <u>Matsui et al.</u>

Therefore, Matsui et al., combined with any of Satoh, Ohuchi, or Riding et al., fails to teach or suggest each and every element recited in claim 13. It actually teaches away from the present invention. Accordingly, no *prima facie* case of obviousness has been made since, in addition to the claimed elements not being disclosed or suggested by the cited references, there is no motivation to combine the references. Finally, the fact that the references teach away from the claimed invention demonstrates that there would be no expectation of success required to sustain an obviousness rejection.

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Applicants therefore respectfully request that the rejection of claims 15-16 under 35 U.S.C. §103(a) be withdrawn.

In view of the foregoing remarks, Applicants respectfully request the reconsideration and reexamination of this application and the timely allowance of the pending claims 13-16.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully Submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: October 17, 2002

Mar & Oloteth Reg No 24, 014 -Richard, V. Burgujian

Reg. No. 31,744

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APPENDIX TO AMENDMENT FILED OCTOBER 17, 2002

Amended claim:

13. (Amended) A method of manufacturing a semiconductor device[adhering on an adhesive side of an adhesive tape chips separated by dicing a wafer, and sequentially peeling the chips off the adhesive tape to be carried], comprising:

adhering on an adhesive side of an adhesive tape chips separated by dicing a wafer; and

repeating a step of peeling a chip off the adhesive tape to sequentially peel the chips off the adhesive tape, wherein the step of peeling a chip off the adhesive tape comprises:

thrusting the chip[s] [by] using pins from a back side of the adhesive tape with the adhesive tape between the chip[s] and the pins, and keeping the pins at a peak position for an amount of time to facilitate peeling the chip off the adhesive tape, wherein the pins do not pierce the adhesive tape;

[absorbing the chips by] descending a collet from the adhesive side of the adhesive tape to contact <u>and suck</u> the chip[s] when the chip[s] [are] is peeled off the adhesive tape; and

[causing the pins to keep thrusting, and] picking the chip[s] up by ascending the collet [after the chips are peeled off the adhesive tape, in order to be carried the chips to a subsequent process stage].

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